

“How I find more time to play golf and kill fewer design engineers each week”

By: Doug Parker, NCE

Sponsored By:





The What, Where, When And Who

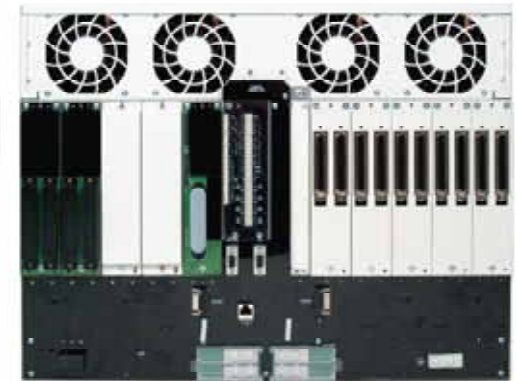


Located In Huntsville, AL

Multiservice Access and Aggregation

Total Access 5000

Total Access Systems



NetVanta® Routers

Solutions to Empower Your Network



Things We Typically Review To Cover EMC:

- Schematic Concerns
- Layer Stackup
- Mechanical Concerns
- Power Supply Layout
- Electrostatic Discharge Protection
- Clock Line Trace Length
- Clock Line Via Count
- Traces Near Plane Edges
- Reference Plane Changes
- Return Current Path Discontinuities
- Signal Guard Traces
- Signal Guard Trace Via Spacing
- Grounding Vias Along Ground Plane Outline
- Filter Component Placement
- Decoupling Capacitor Placement
- Differential Signal Mismatch
- Cross Talk
- Power / Ground Plane Resonance Analysis

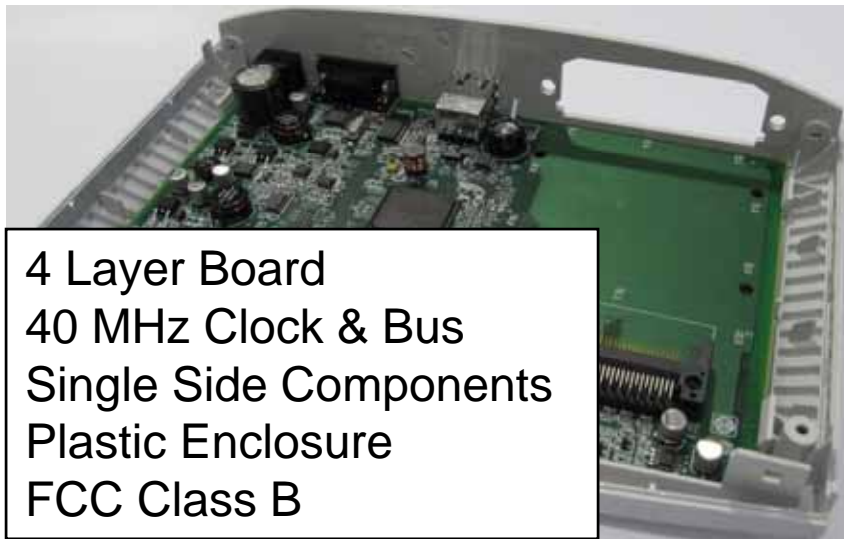
**4 To 8 Hour Review
Manually**

**1 To 3 Hour Review
With**

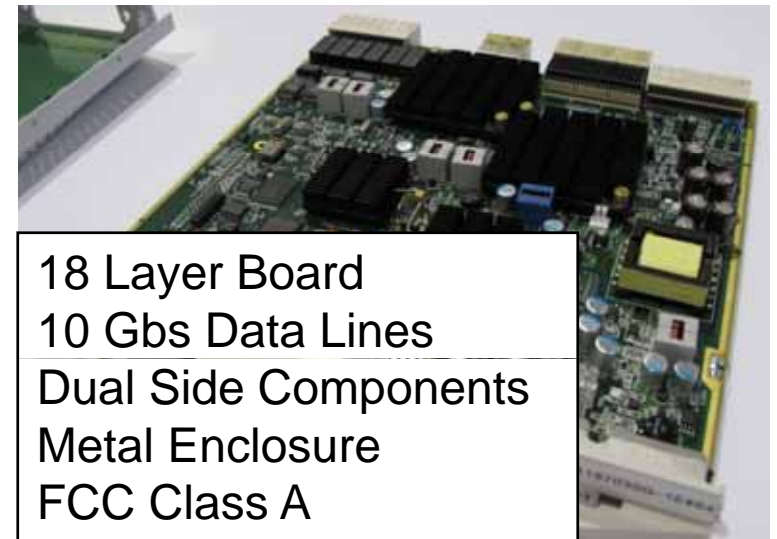




A Broad Range Of Products

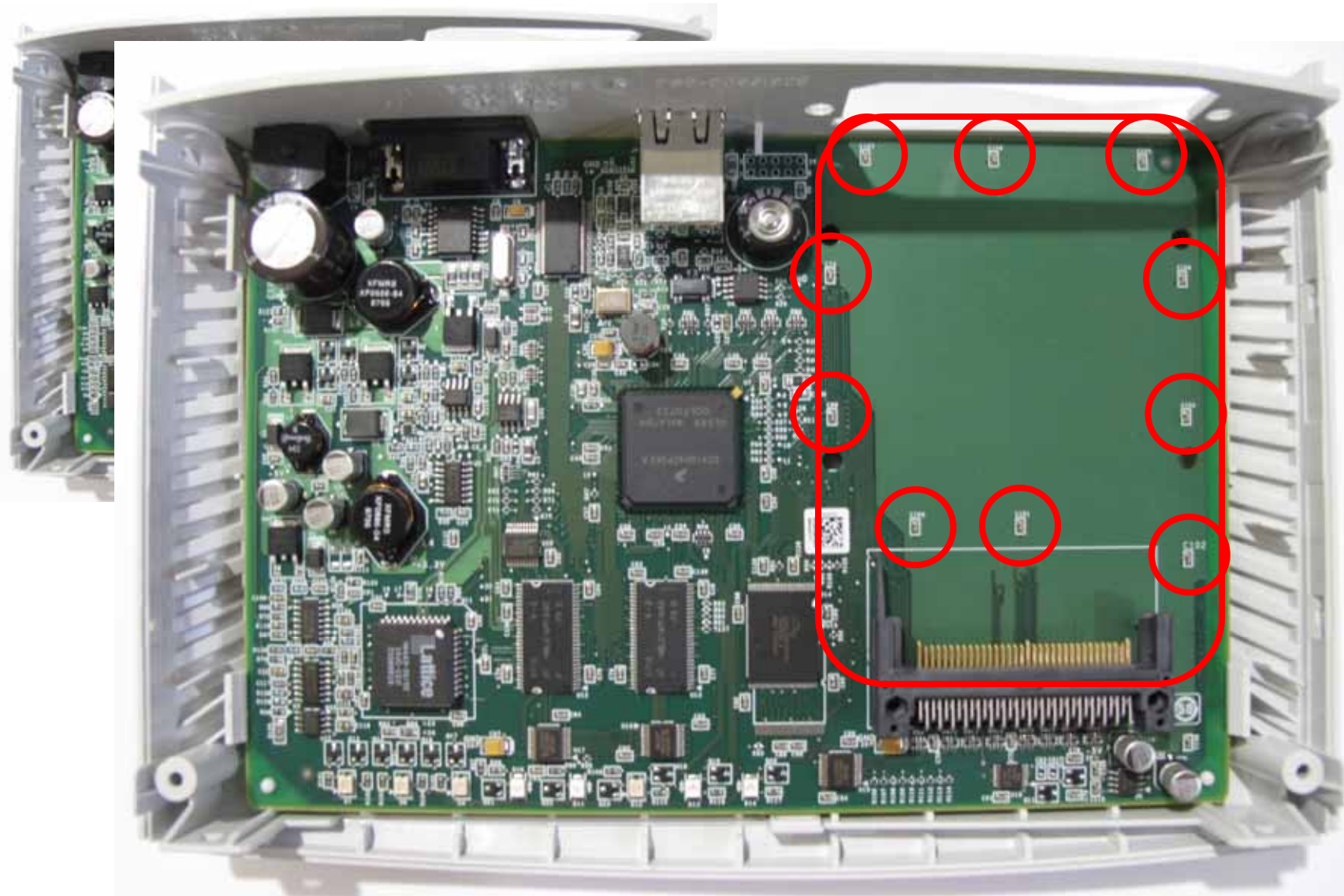


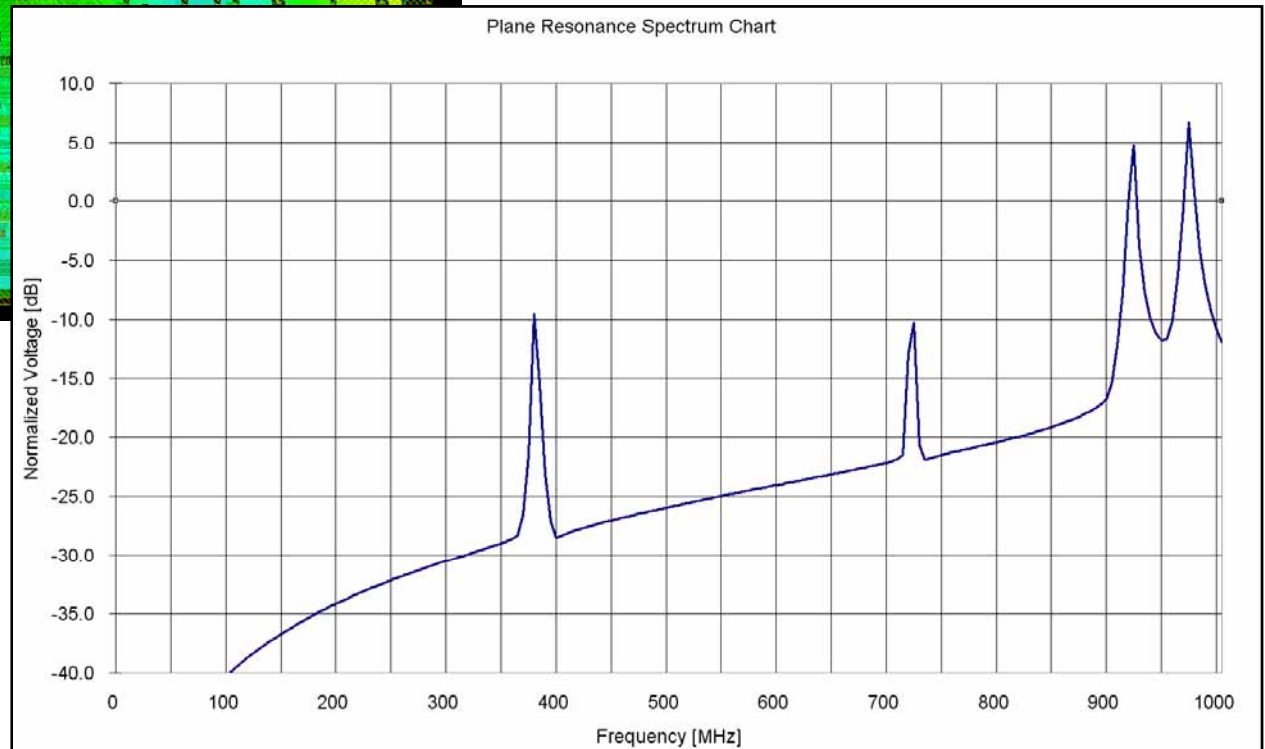
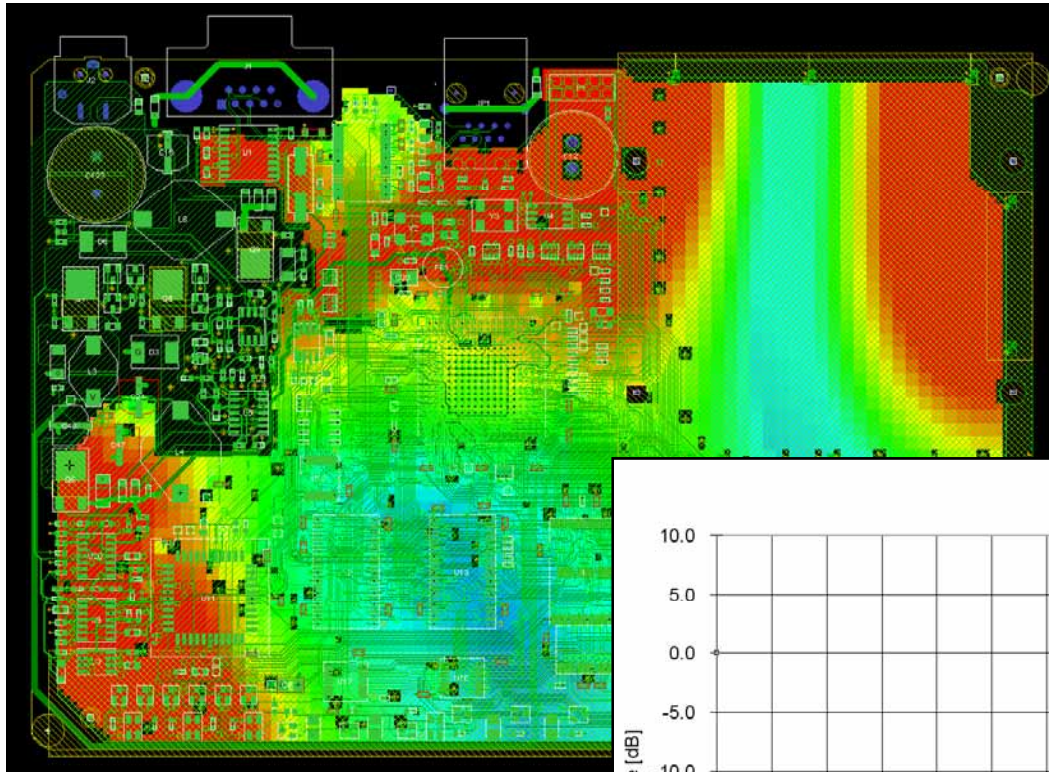
4 Layer Board
40 MHz Clock & Bus
Single Side Components
Plastic Enclosure
FCC Class B

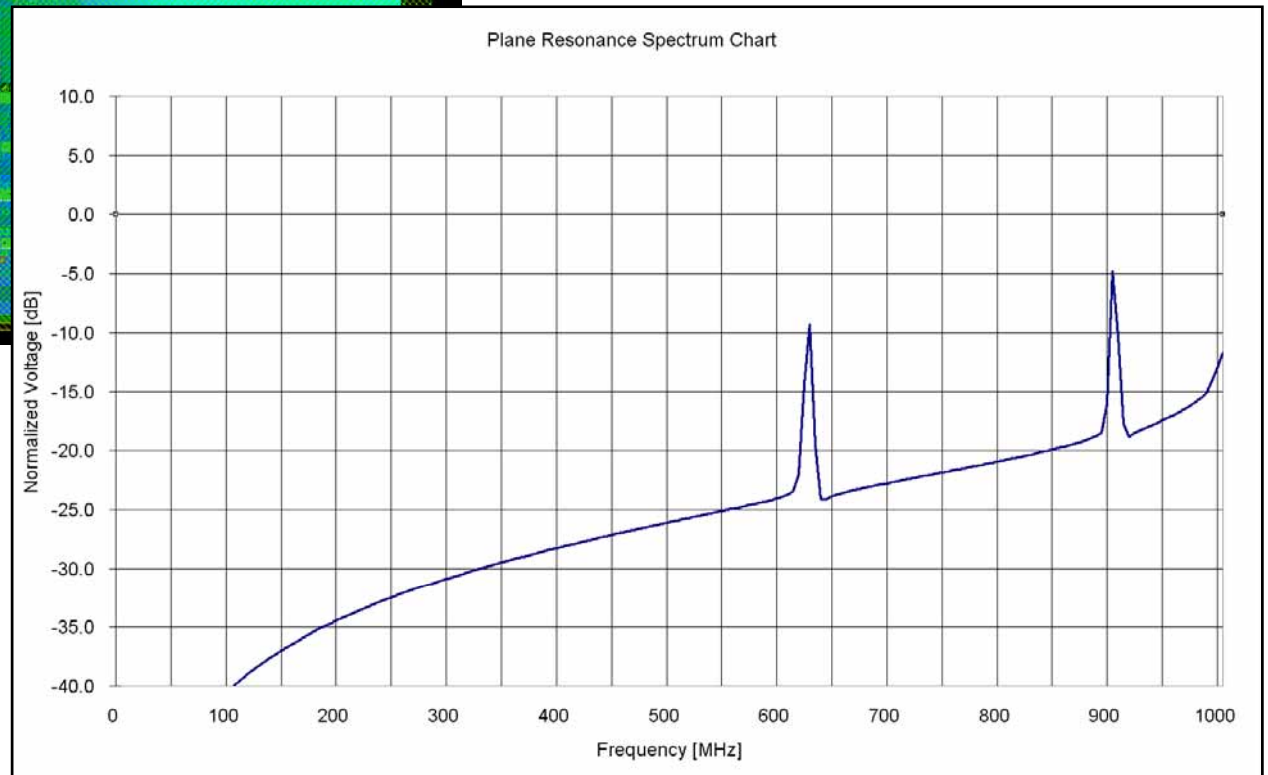
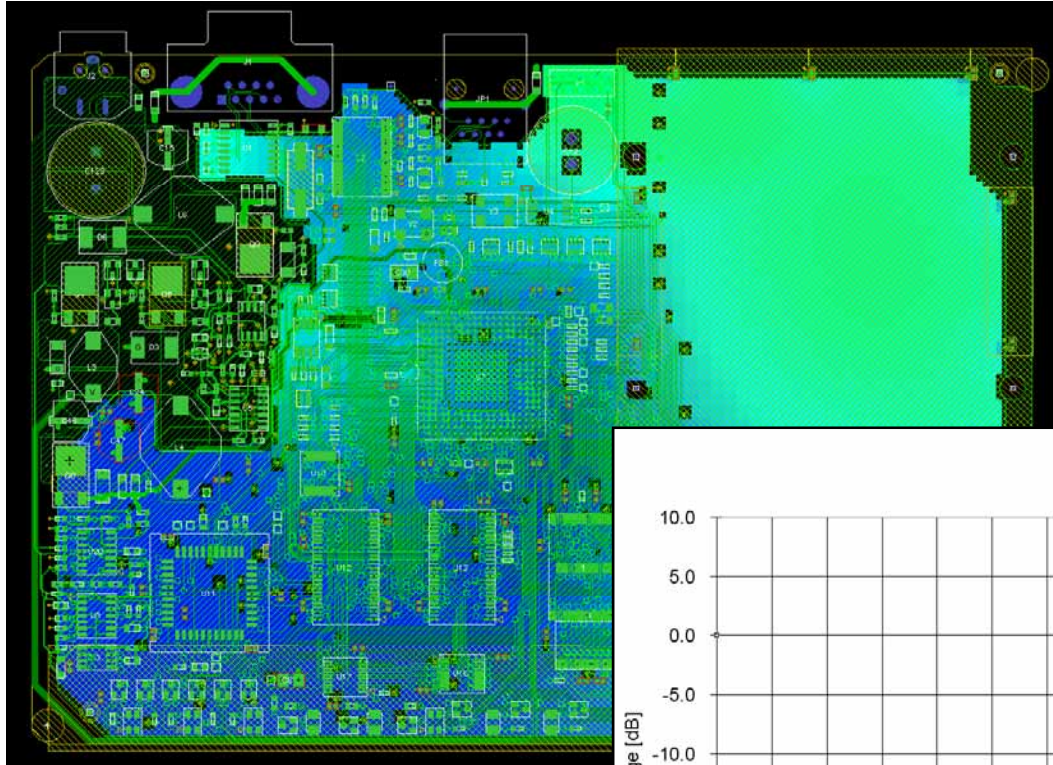


18 Layer Board
10 Gbs Data Lines
Dual Side Components
Metal Enclosure
FCC Class A

Four Layer Board In Plastic Box







**40 MHz Clock
Harmonics
(MHz)**

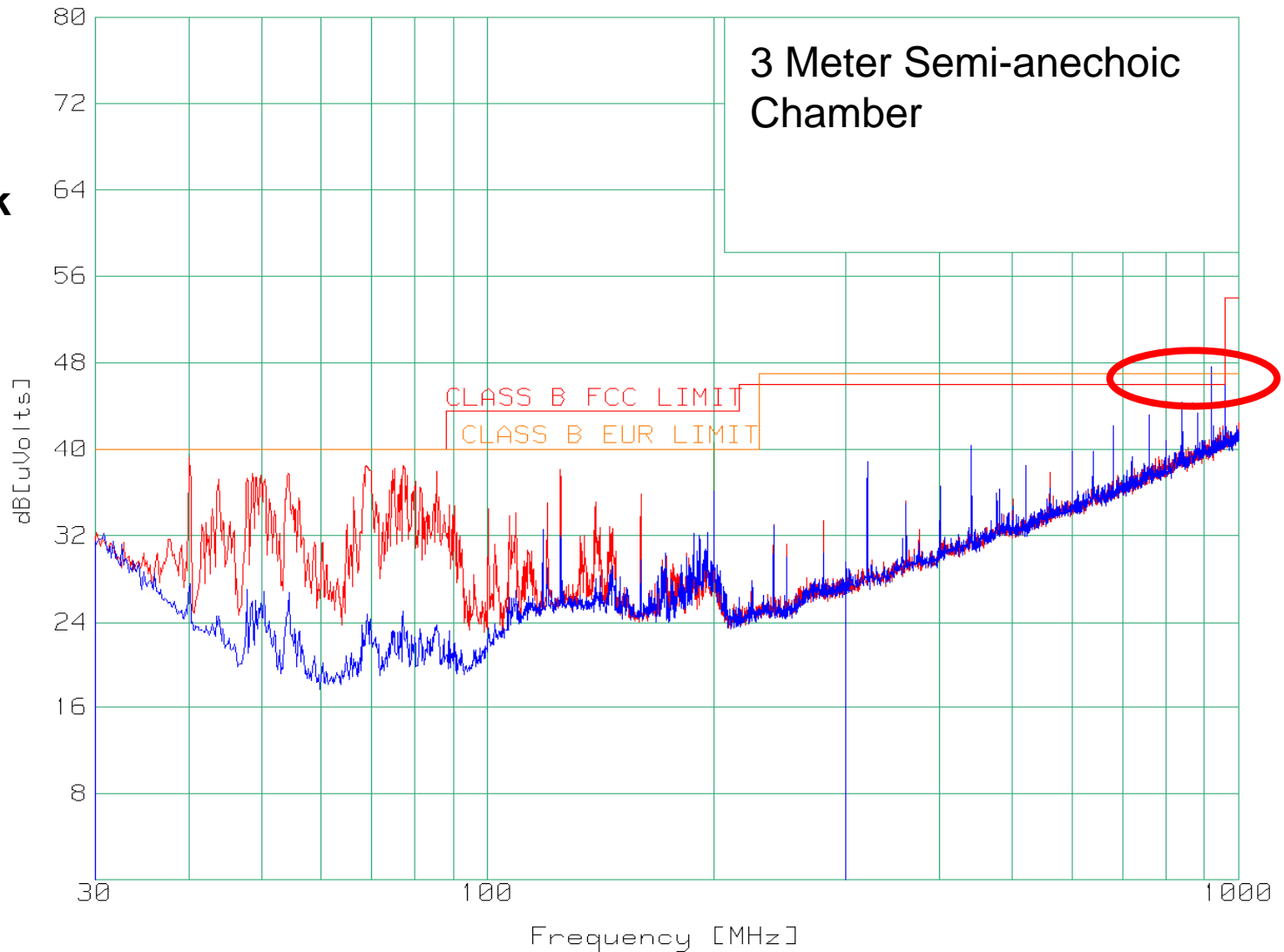
800

840

880

920

960



Before

After

**40 MHz Clock
Harmonics
(MHz)**

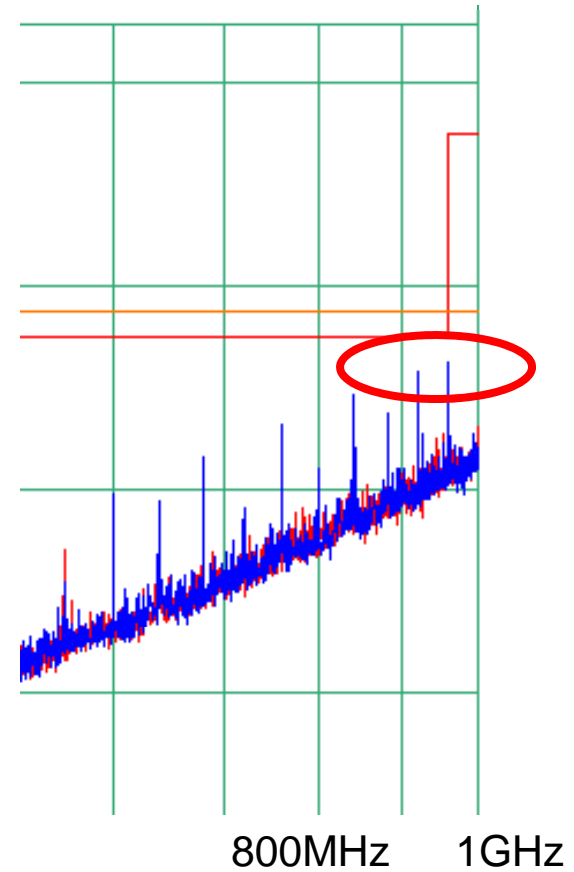
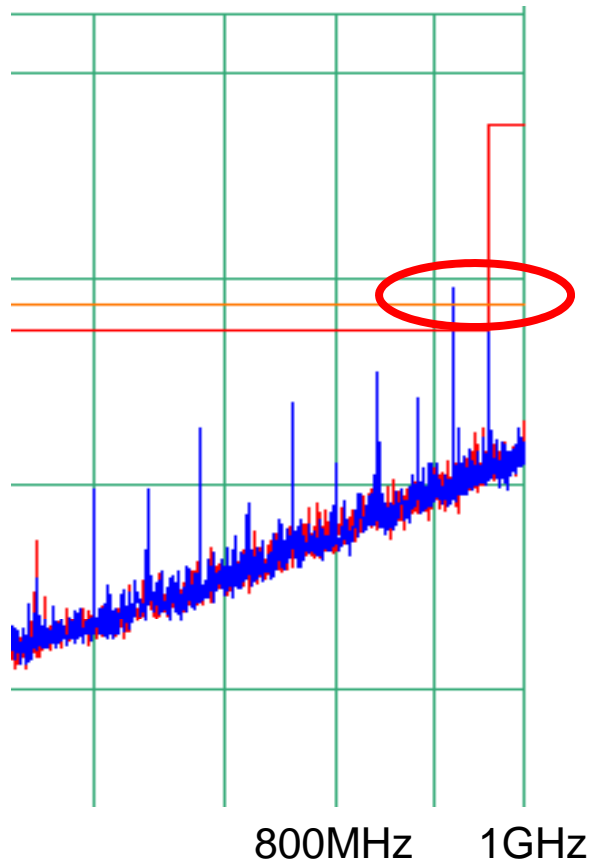
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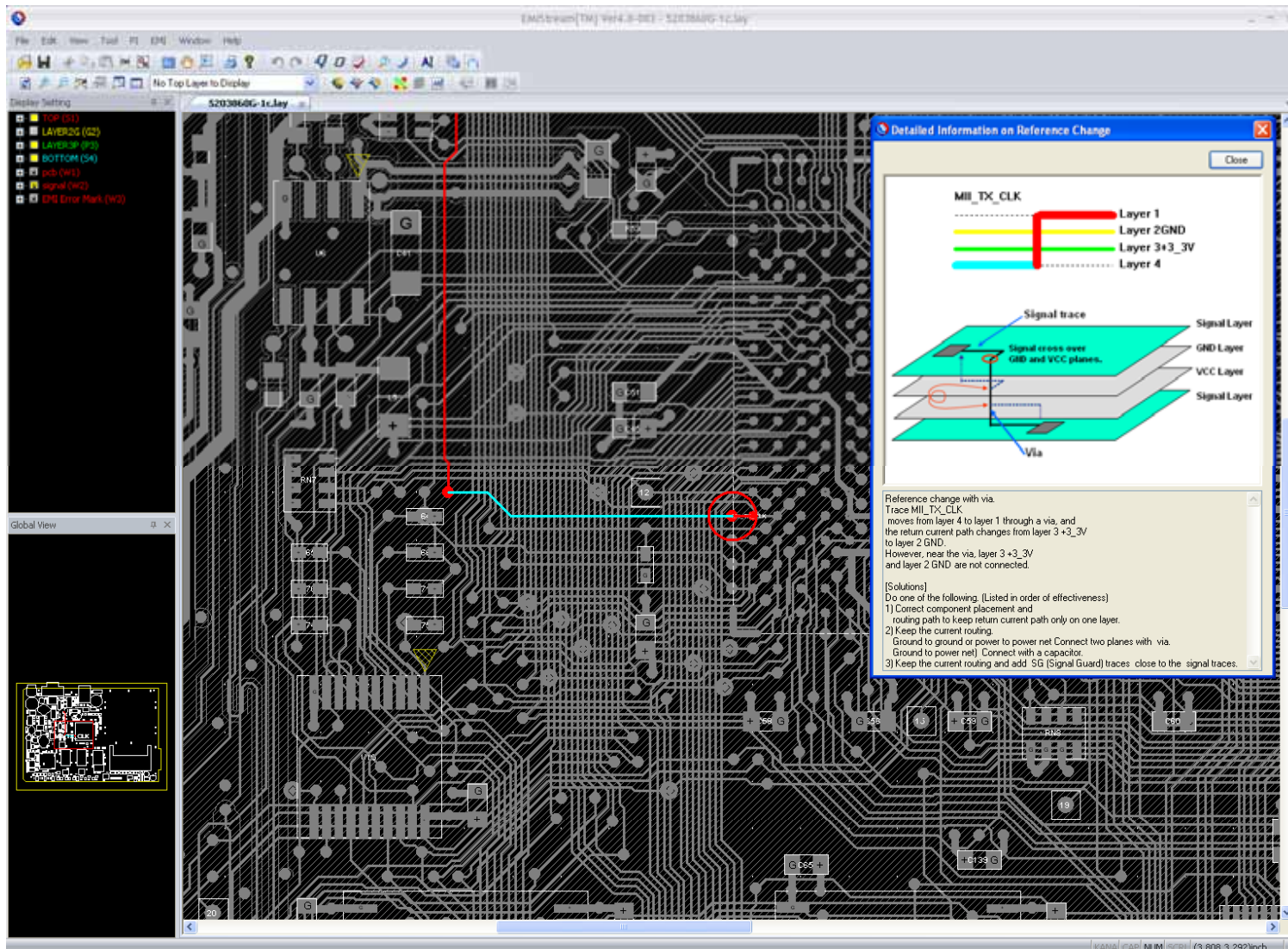
840

880

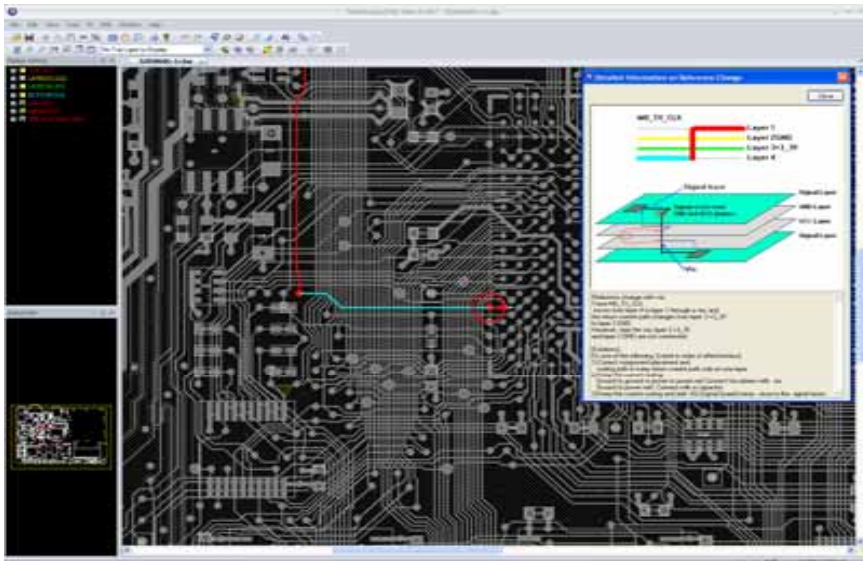
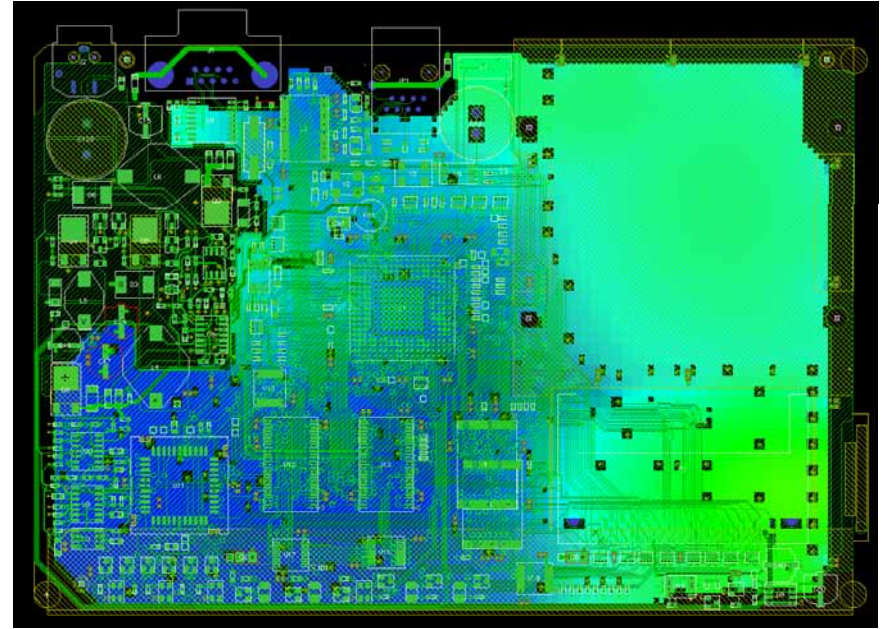
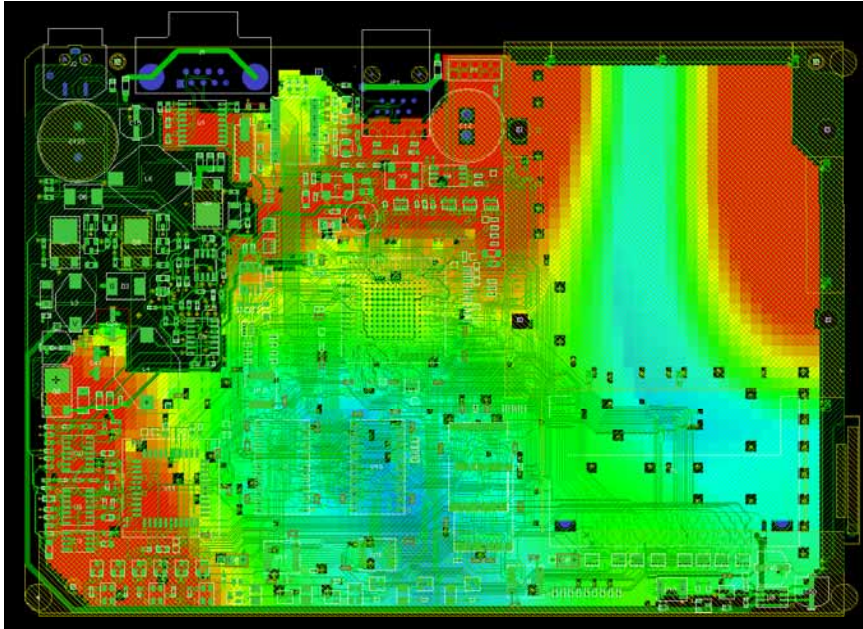
920

960





**Return
Current
Violation**



They say

“A pictures worth a thousand words”

You can add:

4 hrs of arguing with a design engineer

10 cents on your bill of materials

a whole lot of debug time at the lab